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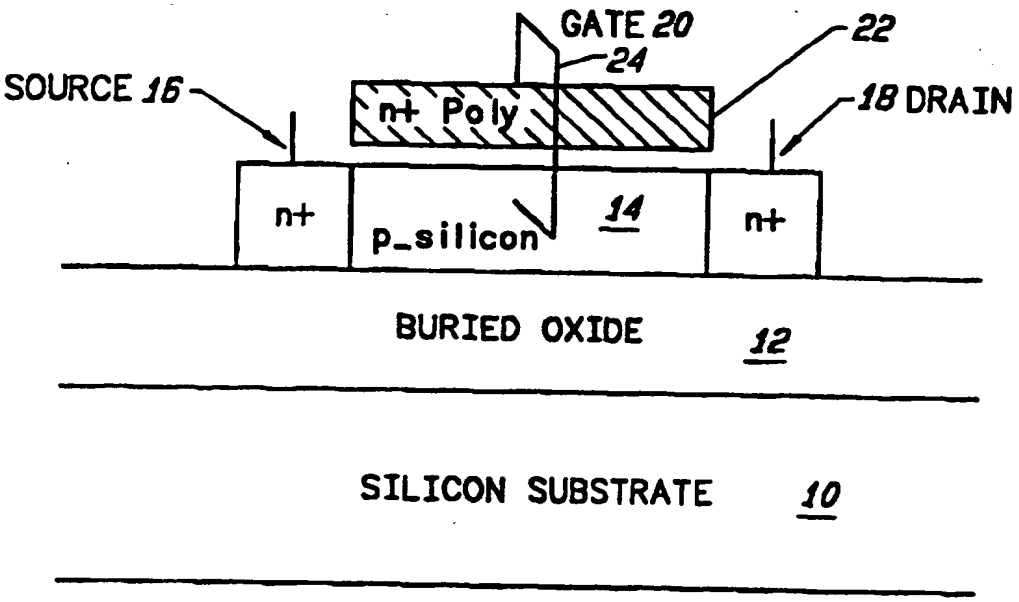

(57) Abstract

A dynamic threshold voltage IGFET such as a MOSFET is operable at voltages of 0.6 volt or less. The threshold voltage of the transistor is reduced to zero volt or less by interconnecting the gate contact (20) and the device body (14) in which the voltage controlled channel is located. Several efficient connections using through hole plating or polycrystalline silicon gate extension are disclosed. A higher power supply voltage can be used by interconnecting the gate and device body through a smaller MOSFET.

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DYNAMIC THRESHOLD VOLTAGE MOSFET FOR ULTRA-LOW VOLTAGE OPERATION

BACKGROUND OF THE INVENTION

This invention relates generally to insulated gate field effect transistors (IGFETs) such as MOSFET devices and integrated circuits, and more particularly the invention is directed to such devices and integrated circuits which can operate at an ultra-low voltage of 0.6 volt or less.

During the past few years, demand for high performance and low power digital systems has grown very rapidly. Several factors have contributed to this fast growth. First, laptop and notebook computers, and personal communication systems have gained popularity. Consequently, portable applications that traditionally required a modest performance (such as wrist watches and calculators) are now dominated by devices that demand a very high performance. The demand for portability of these new systems limits their weight and size, placing a severe constraint on their power dissipation. Second, speed, density and size of non-portable CMOS based systems have increased tremendously in recent years. Thus, power consumption, which was not a concern in these systems, now is becoming a critical parameter.

The main approach for reducing power has relied on power supply scaling. This is due to the fact that in CMOS digital circuits delivered power is proportional to the square of power supply voltage. Since power supply reduction below three times the threshold voltage ($3V_t$) will degrade circuit speed significantly, scaling of power supply should be accompanied by threshold voltage reduction. However, the lower limit for threshold voltage is set by the amount of off-state leakage current that can be tolerated (due to standby power consideration in static circuits, and avoidance of failure in dynamic circuits and memory arrays). It is seen

that if regular MOSFETs are used, a lower bound for power supply voltage becomes inevitable.

Silicon-on-insulator (SOI) technology offers much promise for ultra large scale integrated circuits using sub-micron gate technology. This technology employs a layer of semiconductor material overlying an insulation layer on a supporting bulk wafer. The structure can be formed by a number of well-known techniques, such as zone melting and recrystallization (ZMR), separation by implanted oxygen (SIMOX), and Bonded and Etchback (BESOI). Typically, the structure comprises a film of monocrystalline silicon on a buried layer of silicon oxide in a monocrystalline silicon substrate.

The bulk silicon material in which the channel of a MOSFET device is formed is typically grounded or connected to the source region of the device. However, in SOI MOSFETs the monocrystalline silicon film is often unbiased or floating. Heretofore, a SOI MOSFET has been operated as a lateral bipolar transistor by connecting the silicon film to the gate and exploiting the extra current produced by the device. However, this operation requires the body voltage to be larger than 0.6 volt. And since the current gain of the bipolar device is small, the extra drain (collector) current comes at the cost of excessive input (base) current, which contributes to standby current. This is contrary to a low-power operation.

SUMMARY OF THE INVENTION

In accordance with the invention, an IGFET such as a MOSFET formed in an SOI structure includes a gate to body connection to reduce turn-on voltage (V_t) and extend the lower bound of power supply voltage to an ultra-low level (*i.e.*, 0.6 volt or less). The body contact can be provided by metal through a contact window in a polysilicon gate to the underlying film. Alternatively, the polysilicon gate can contact the silicon film directly through a contact window in the gate insulation. Also, separate contacts can be provided

to the polysilicon gate, and to the body. These contacts can be shorted by the first-layer metal.

In another embodiment of the invention, an external bias generation circuit is provided so that the low threshold device can operate above 0.6 volt supply voltage. In this embodiment, a small field effect transistor provides forward body bias for a larger transistor. The small transistor limits the forward body bias to only 0.6 volt regardless of power supply voltage, thus V_{dd} will no longer be limited to 0.6 volt. This embodiment is especially useful in circuits where large transistors are needed, such as in clock drivers and large buffers. The purpose of this connection is that the large transistor will have a much higher current drive than that of a regular transistor with the same size.

The invention and objects and features thereof will be more readily apparent from the following description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic representation of an SOI MOSFET in accordance with the invention.

FIGS. 2A and 2B are a top view and a side view in section of one embodiment of the invention.

FIGS. 3A, 3B are a top view and a side view in section of another embodiment of the invention.

FIGS. 4A, 4B are a top view and a side view in section of another embodiment of the invention.

FIG. 5 is a top view of another embodiment of the invention.

FIG. 6 is a side view in section of another embodiment of the invention.

FIG. 7 is a schematic representation of the invention embodied in a conventional bulk device.

FIG. 8 is a plot of threshold voltage of an SOI NMOSFET as a function of body-source forward bias.

FIG. 9 is a plot of subthreshold characteristics of SOI NMOSFET and PMOSFET with body grounded and body tied to the gate.

FIG. 10 is a plot of mobility for a DTMOSFET and for a conventional MOSFET.

FIG. 11 is a plot of drain current of an SOI NMOSFET operated as a DTMOSFET and as a conventional MOSFET.

FIG. 12 is a plot of delay of a 101-stage ring oscillator with the PMOS and NMOS devices in the ring being DTMOS with T_{ox} = 10 nm, Leff = 0.3 μm, and V_{to} = 0.6V.

FIG. 13 is a plot of DTMOS inverter DC transfer characteristics.

FIG. 14 is a plot comparing floating and grounded body SOI MOSFETs.

FIG. 15 is a schematic of an alternative embodiment of a DTMOS device.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Dynamic threshold MOS (DTMOS) devices in accordance with the invention have been fabricated on Silicon-On Insulator (SOI) substrates. Mesa active islands (MESA) were created by plasma-etching a nitride/oxide/silicon stack stopping at buried oxide. P+ polysilicon gate was used for PMOSFETs and N+ for NMOSFETs. Oxygen plasma "ashing" was done to the gate photoresist to achieve effective channel length down to 0.2μm. A four-terminal layout was used to provide separate source, drain, gate, and body contacts. In addition to the four-terminal layout, devices with local gate-to-body connections were also fabricated as illustrated in FIG. 1 and FIG. 2.

In FIGS. 1 and 2, silicon substrate 10 has a buried oxide layer 12 formed therein with P- silicon film 14 on layer 12. N+ source 16 and N+ drain 18 are formed in film 14 with a gate electrode 20 formed over gate insulation 22 and the channel region between source 16 and drain 18. Gate 20 and film 14 are interconnected by connection 24. For NMOS, this connection uses an oversized metal-to-P+ contact window aligned over a "hole" in the poly gate. The metal shorts the gate and the P+ region. This ensures that the body-to-gate connection does not come at the expense of a significantly

larger device area. A similar structure is used for PMOS device except that the P+ region is replaced by an N+ region.

Other connection methods that rely on metal shorting the polysilicon gate to the body are illustrated in FIGS. 3, 4, and 5. Like elements in FIGS. 1-7 have the same reference numerals. In the regions where polysilicon gate will be connected to the body, an oxide thicker than the gate oxide may be used to minimize the overlap capacitance. Specifically, in FIGS. 2-5, this region corresponds to the area where polysilicon is next to or over the P+ silicon film.

It is not necessary to use metal for shorting the body to the gate, as a buried contact can be exploited, as illustrated in FIG. 6. After gate oxidation, a thin layer of polysilicon (approximately 20nm-30nm) is deposited. Next, a new mask is used to make a contact window by etching the polysilicon layer and the underlying oxide in the selected area. Subsequently, a thick layer of poly is deposited. This polysilicon layer will be shorted to the silicon film directly in the contact window. Obviously, the silicon region where the contact is made has to be doped P+ (as shown in FIG. 6), so that an ohmic contact to the body is formed.

In the DTMOS in accordance with the invention, the floating body and the gate of the Silicon-On-Insulator (SOI) MOSFET are tied together. A large improvement over regular MOSFET can be achieved when gate and body voltages are kept below 0.6V. This also ensures that base current will stay negligible. The same idea can be used in bulk devices by connecting the well to the gate, illustrated in FIG. 7. However, particular advantage is realized in SOI, where base current and capacitances are appreciably reduced because of very small junction areas. The data presented here pertain only to the SOI devices.

FIG. 8 illustrates the NMOS behavior, with a separate terminal sued to control the body voltage. The threshold voltage at zero body bias is denoted by V_{to}. Body bias effect is normally considered in the reverse bias regime, where threshold voltage increases as body-to-source reverse bias is made larger. DTMOS is operated in the exact opposite

regime. Namely, we "forward bias" the body-source junction (at less than 0.6V), forcing the threshold voltage to drop.

Specifically, this forward bias effect is achieved by connecting the gate to the body. This is shown as the $V_{gs} = V_{bs}$ line in FIG. 8. In FIG. 8, Technology-A has T_{ox} = 10nm, Na = 2.0 x $10^{17}cm^{-3}$, and for Technology-B T_{ox} = 6.4nm and Na = 2.3 x $10^{17}cm^{-3}$. A hypothetical case with Na = 6 x $10^{17}cm^{-3}$ and V_{fb} = -1.25V is shown as the dashed line. The intersect of the V_t curve and the $V_{gs} = V_{bs}$ line determines the point where gate and threshold voltages become identical. This point, which is marked as V_{tf}, is the DTMOS threshold voltage. This lower threshold voltage does not come at the expense of higher off-state leakage current, because at $V_{bs} = V_{gs} = 0$, DTMOS and a conventional device have the same V_t. In fact, they are identical in all respects and consequently have the same leakage. This is clearly seen in FIG. 9. Reduced V_{tf} compared to V_{to} is attained through a theoretically ideal subthreshold swing of 60mV/dec. FIG. 9 demonstrates this for PMOS and NMOS devices operated in DTMOS mode and in regular mode. Subthreshold swing is 80mV/dec in the regular devices. The ideal 60mV/dec swing in DTMOS is achieved due to the fact that gate (body) voltage is directly applied to the body, rather than being capacitively coupled.

This is not the only improvement. As the gate of DTMOS is raised above V_{tf}, threshold voltage drops further. The threshold voltage reduction continues until $V_{gs} = V_{bs}$ reaches $2\Phi_b$, and threshold voltage reaches its minimum value of $V_{t,min} = 2\Phi_b + V_{fb}$. For example, for technology-B in FIG. 8, at $V_{gs} = V_{bs}$ = 0.6V, V_t = 0.18V compared to V_{to} = 0.4V. We have included models fitting the experimental data in FIG. 8. To obtain the sharpest curve (and hence the maximum V_t reduction), the highest acceptable channel doping should be used. V_{tf} then can be adjusted to the desired value by a gate material that gives large and negative flat band voltage. A hypothetical case demonstrating this concept is shown in FIG. 8, with doping = 6 x $10^{17}cm^{-3}$ and V_{fb} = 1.25V. Materials with work functions in the range of 3.4eV - 3.8eV such as magnesium will be suitable for the gate. A gate material with

a small work function should be used with NMOSFETs and gate material with a large work function should be used for PMOSFETs.

In DTMOS operation, the upper bound for applied $V_{gs} = V_{bs}$ is set by the amount of base current that can be tolerated. This is illustrated in FIG. 9, where PMOS and NMOS device body (base) currents are shown. At $V_{gs} = 0.6V$, base currents for both PMOS and NMOS devices are less than $2nA/\mu m$. A further advantage of DTMOS is that its carrier mobility is higher because the depletion charge is reduced and the effective normal field in the channel is lowered. This is illustrated in FIG. 10.

Current drives of DTMOS and regular MOSFET are compared in FIG. 11, for technology-B of FIG. 8. DTMOS drain current is 2.5 times that of the regular device at $V_{gs} = 0.6V$, and 5.5 times that of the regular device at $V_{gs} = 0.3V$.

To further illustrate the suitability of DTMOS for ultra low voltage operation, 101-stage ring oscillators were fabricated using technology-A. FIG. 12 plots the delay of each stage versus power supply. We emphasize that since the threshold voltage of devices used in the ring oscillator were high (technology A), the optimum performance was not achieved. For technology-B, ring oscillators are not available. If the devices based on technology-B are used, the expected delay for the unloaded ring oscillator can be calculated by the following equation:

$$\tau_{pd} = \frac{C}{4} V_{dd} \left(\frac{1}{I_{dsatn}} + \frac{1}{I_{dsapt}} \right).$$

This is shown as solid squares in FIG. 12, where C = 200fF is used for $W_n = 5\mu m$ and $W_p = 10\mu m$. This value for C was obtained by fitting the equation to the measured τ_{pd} of technology-A. The inverter DC transfer characteristics for technology-B is shown in FIG. 13. If we adopt the criteria of noise margin being at least $0.2V_{dd}$, and inverter gain being at least 4, this inverter will stay operational down to $V_{dd} = 0.2V$.

The invention relies on providing the body bias externally, *i.e.*, using the gate voltage to forward bias the body. It is possible to use a self generation scheme to forward bias the body. When the device is ON, as the drain voltage is increased, the impact ionization current can forward bias the source-body junction. More specifically, the minority carriers generated by impact ionization accumulate at the back interface and form a equi-potential plane. Equilibrium is obtained when the number of carriers entering the body equals to that leaving the body via the forward-biased source/body diode. This will lead to a significantly reduced subthreshold swing, and lower threshold voltage. Thus, current drive of the device will be enhanced when $V_{gs} = V_{dd}$ and $V_{ds} = V_{dd}$. The threshold voltage reduction will not occur when the device is OFF, *i.e.*, $V_{gs} = 0$, because drain current will be small and impact ionization current will be negligible. FIG. 14 illustrates the self-generation of forward bias in a SOI MOSFET. This device has a four-terminal layout, with a separate body contact. We have compared the floating body against the grounded body configuration. As seen, in the floating body case, subthreshold swing is reduced and higher current drive is achieved. A similar idea can be exploited in a bulk device if the well is left floating.

When the device body is tied directly to the gate, power supply voltage will be limited to about 0.6V or less. To remove this limitation, an external bias generation circuit as illustrated in Fig. 15 includes a small transistor 30 to provide the forward body bias for a large transistor 32. The small transistor limits the forward body bias to only 0.6V regardless of power supply voltage, thus V_{dd} will no longer be limited to 0.6V. The small transistor can be depletion-mode type or enhancement-mode type, with an appropriate gate voltage. This gate voltage can in fact be designed to be zero, so no extra power supply might be needed. The above scheme works particularly well for circuits where large transistors are needed, such as in clock drivers and large buffers. The small transistor adds negligible overhead, but

provides significant current drive improvement for the large MOSFET.

There has been described several embodiments of a VTMOS device in accordance with the invention. While the invention has been described with reference to the several embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications might occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. For use in an integrated circuit operable at a power supply voltage 0.6 volt or less, a dynamic threshold insulated gate field effect transistor comprising

a semiconductor body region of a first conductivity type and having a surface,

a source region and a drain region of a second conductivity type formed in said semiconductor body region and abutting said surface, said source region and said drain region being spaced apart with a channel region therebetween,

an insulative layer on said surface over said channel region,

a gate contact on said insulative layer and over said channel region, and

a connector interconnecting said gate contact and said semiconductor body region.

2. The transistor as defined by claim 1 wherein said semiconductor body region comprises a doped well of said first conductivity type formed in a semiconductor substrate of opposite conductivity type.

3. The transistor as defined by claim 2 wherein said semiconductor substrate comprises monocrystalline silicon.

4. The transistor as defined by claim 1 wherein said semiconductor body region comprises a silicon film in a silicon on insulator (SOI) structure.

5. The transistor as defined by claim 4 wherein said connector comprises a metal connecting said gate contact to said silicon film through a hole in said gate contact and said insulative layer.

6. The transistor as defined by claim 4 wherein said connector comprises a metal overlapping said gate contact and an exposed portion of said silicon film extending beyond an edge of said gate contact.

7. The transistor as defined by claim 4 wherein said gate contact comprises doped polycrystalline silicon and said connector comprises an extension of said doped polycrystalline silicon contacting said silicon film.

8. The transistor as defined by claim 4 wherein said transistor is an NMOSFET and said gate contact comprises a metal having a small work function.

9. The transistor as defined by claim 4 wherein said transistor is a PMOSFET and said gate contact comprises a metal having a large work function.

10. The transistor as defined by claim 1 wherein said transistor is an NMOSFET and said gate contact comprises a metal having a small work function.

11. The transistor as defined by claim 1 wherein said transistor is a PMOSFET and said gate contact comprises a metal having a large work function.

12. The transistor as defined by claim 1 wherein said insulated gate field effect transistor comprises a MOSFET.

13. A dynamic threshold insulated gate field effect device comprising

a first transistor having a source, a drain, a channel region between said source and said drain, and a gate contact overlying said channel region,

a second transistor having a source, a drain, a channel region between said source and said drain, and a gate contact overlying said channel region,

means interconnecting said drain of said second transistor to said gate of said first transistor,

means interconnecting said source of said second transistor to said body region of said first transistor, and

means for biasing said gate contact of said second transistor with an appropriate gate voltage.

14. The device as defined by claim 13 wherein said first transistor is larger than said second transistor.

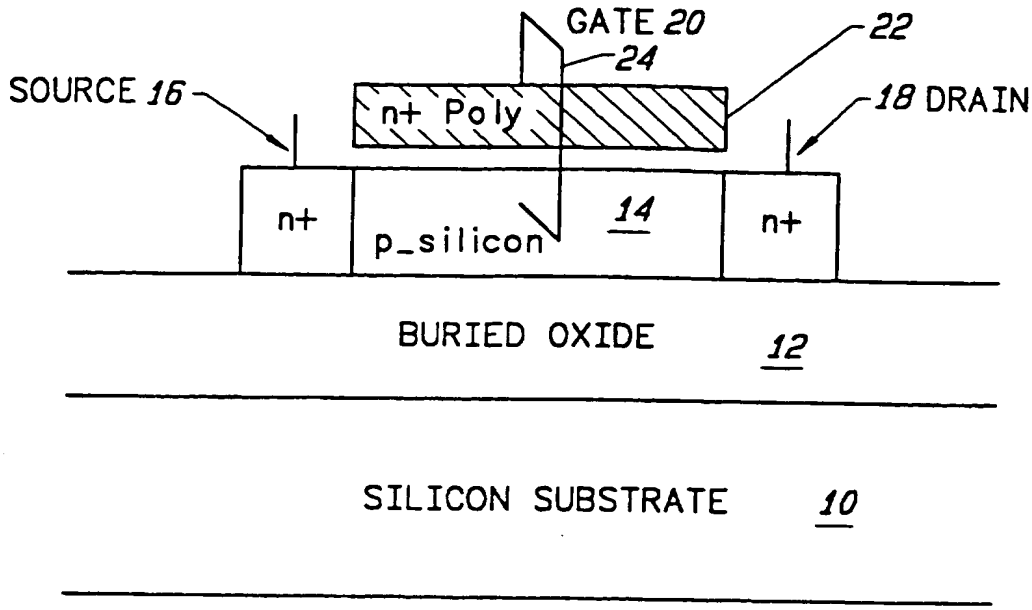


FIG. 1

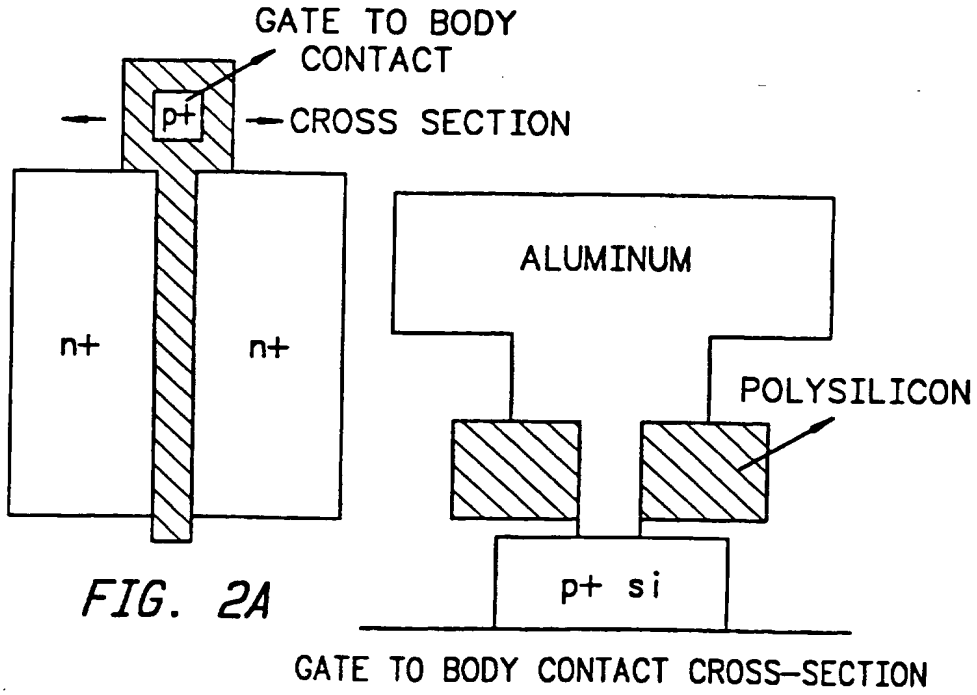


FIG. 2A

FIG. 2B

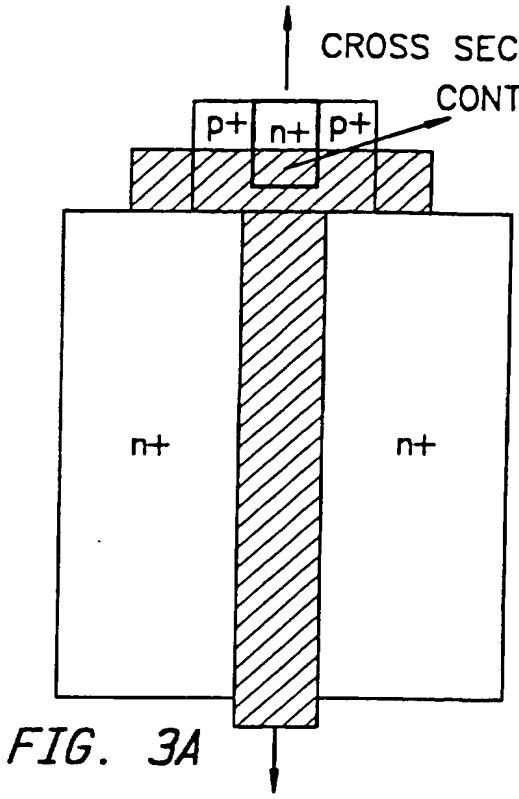
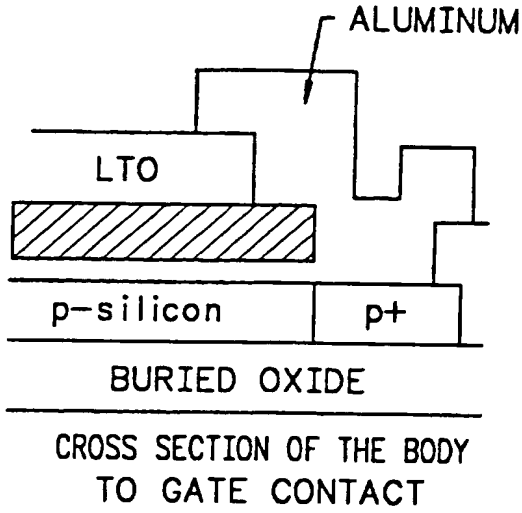


FIG. 3A



CROSS SECTION OF THE BODY TO GATE CONTACT

FIG. 3B

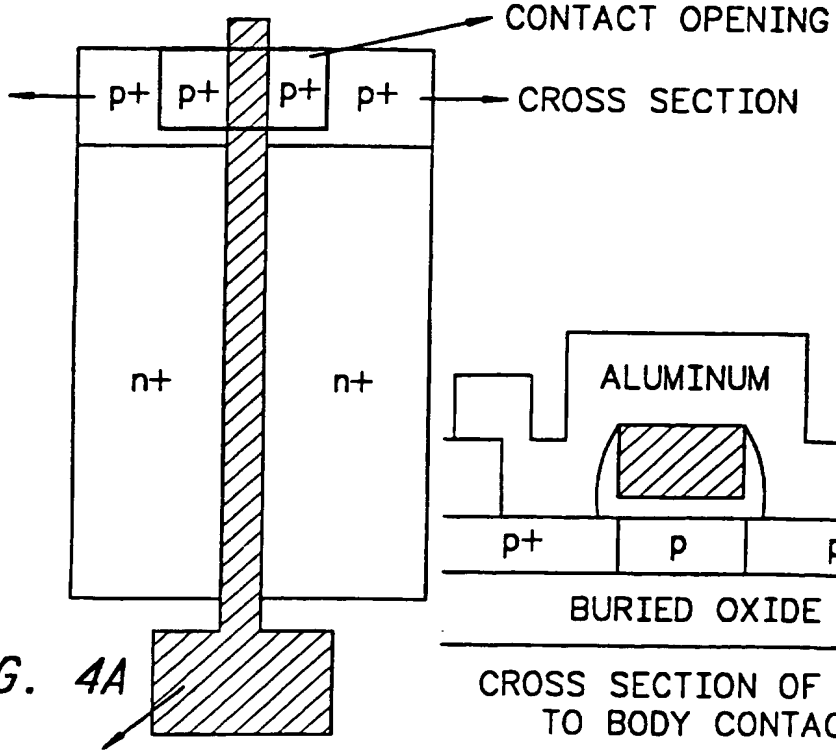


FIG. 4A

CROSS SECTION OF GATE TO BODY CONTACT

FIG. 4B

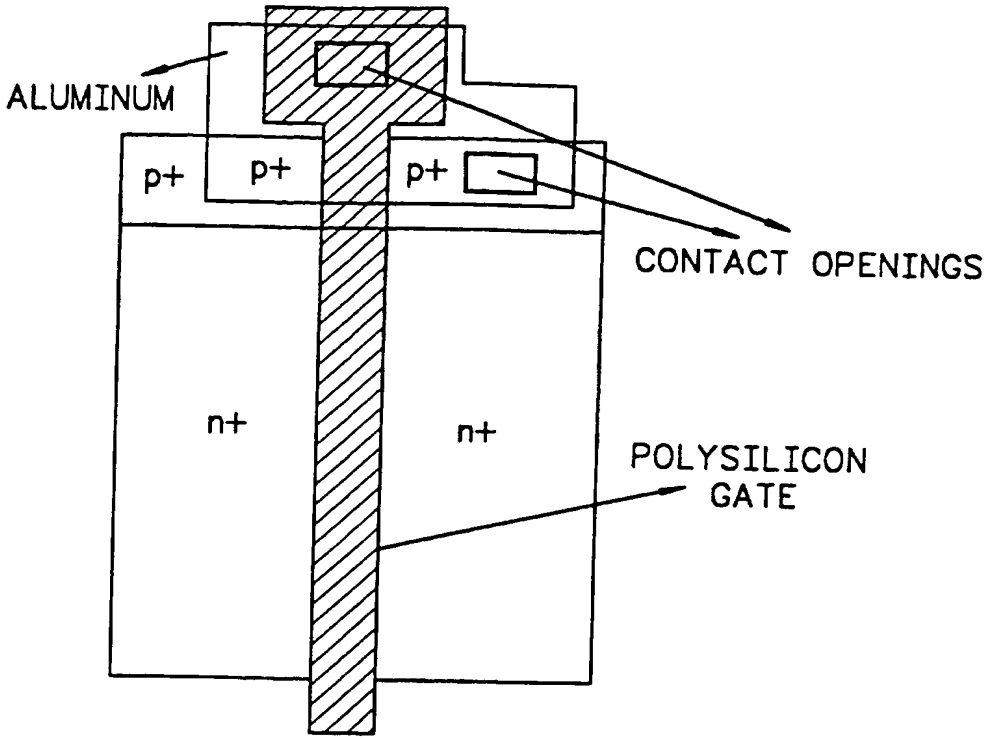


FIG. 5

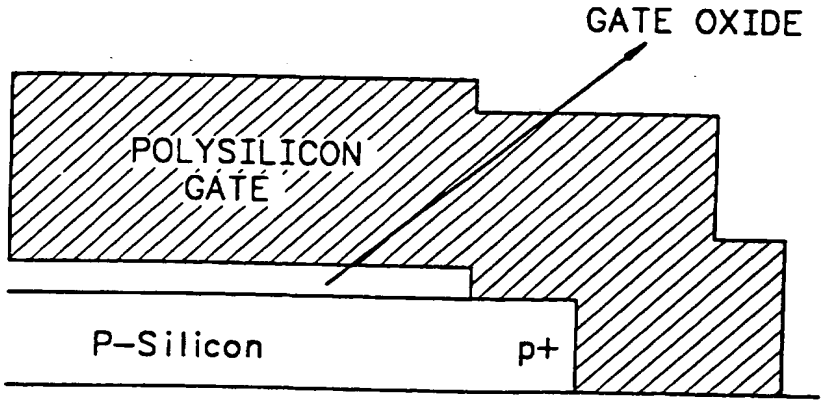


FIG. 6

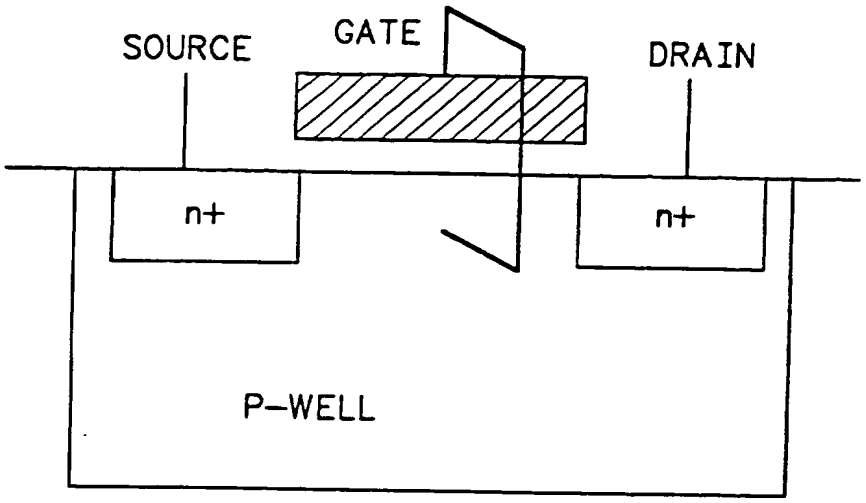


FIG. 7

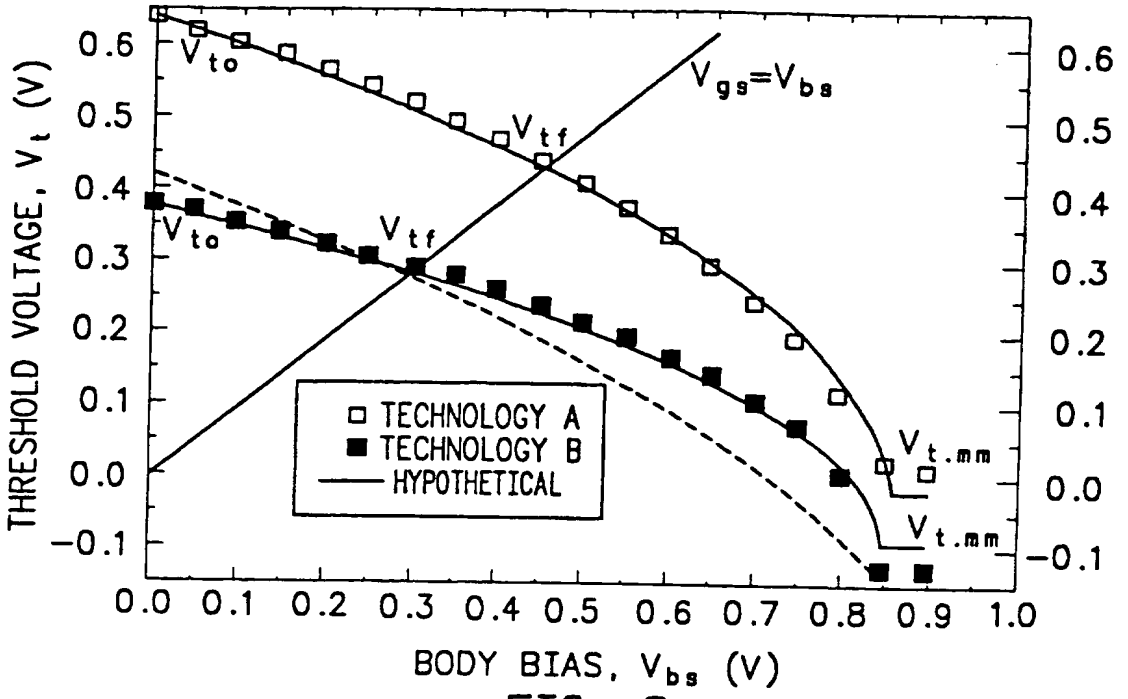


FIG. 8

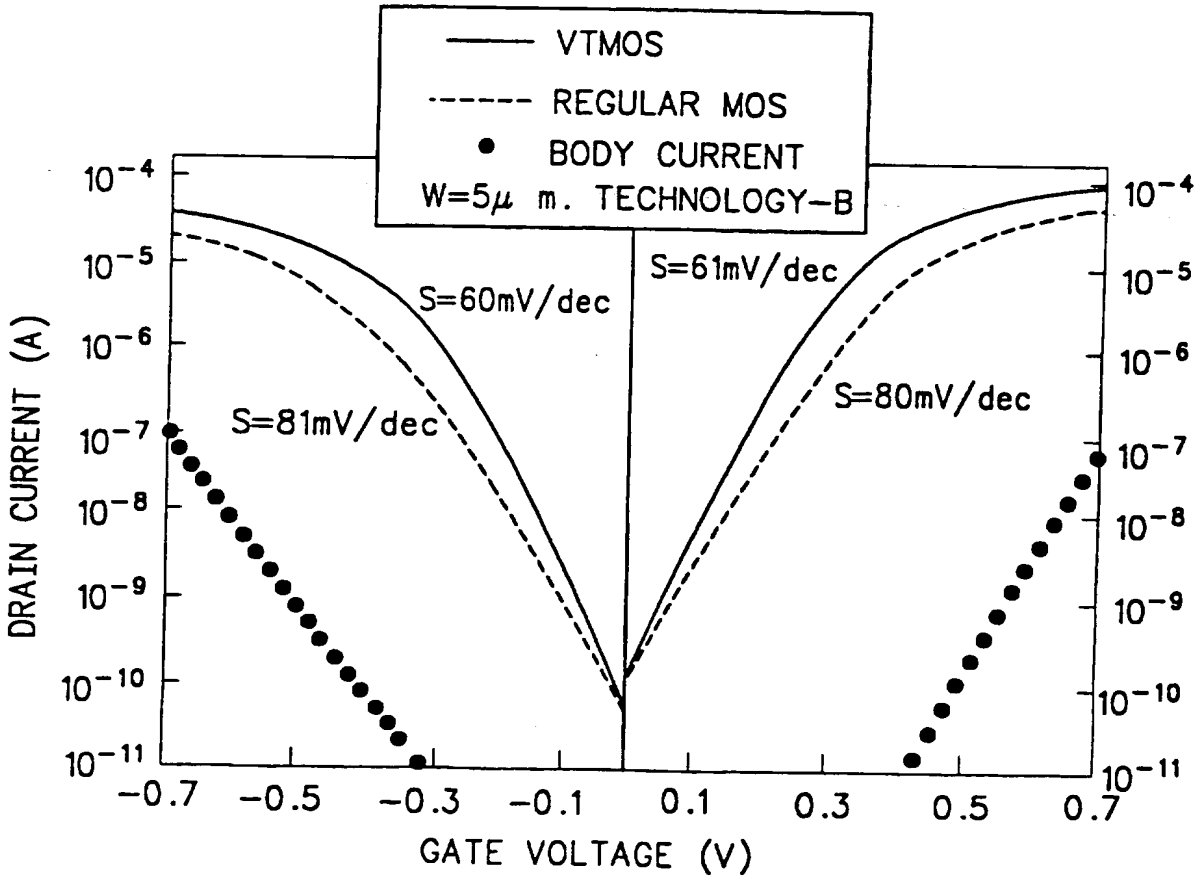


FIG. 9

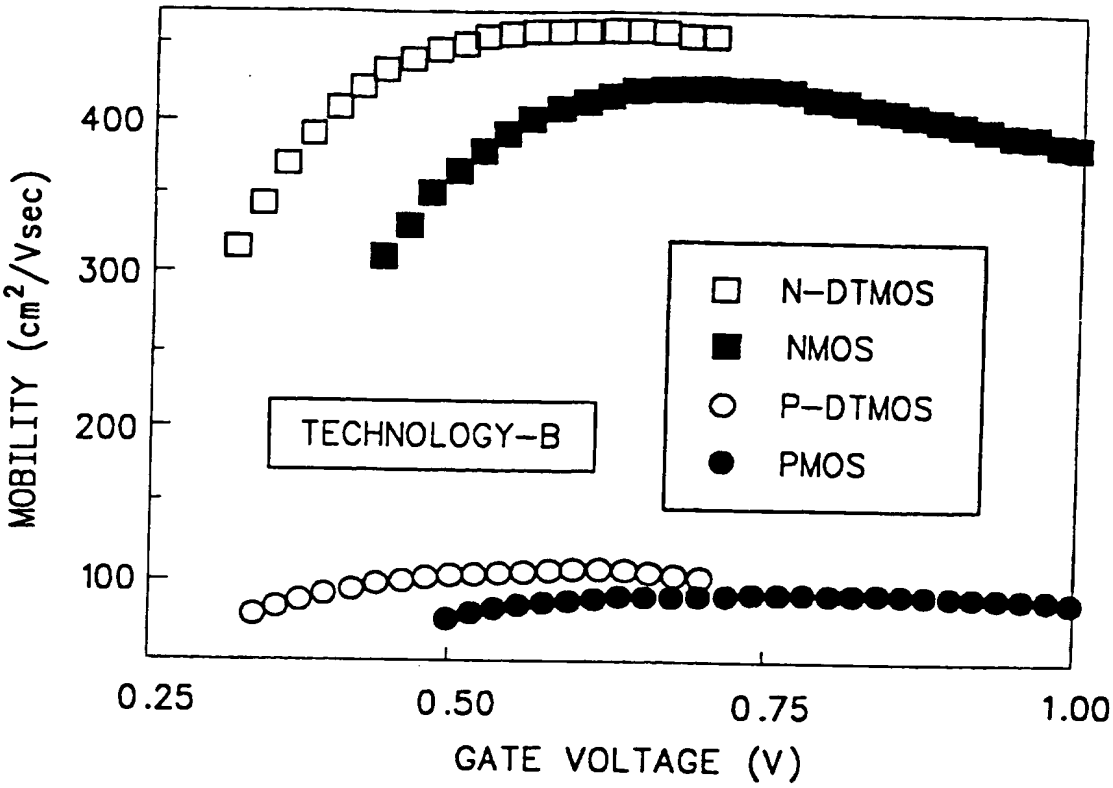


FIG. 10

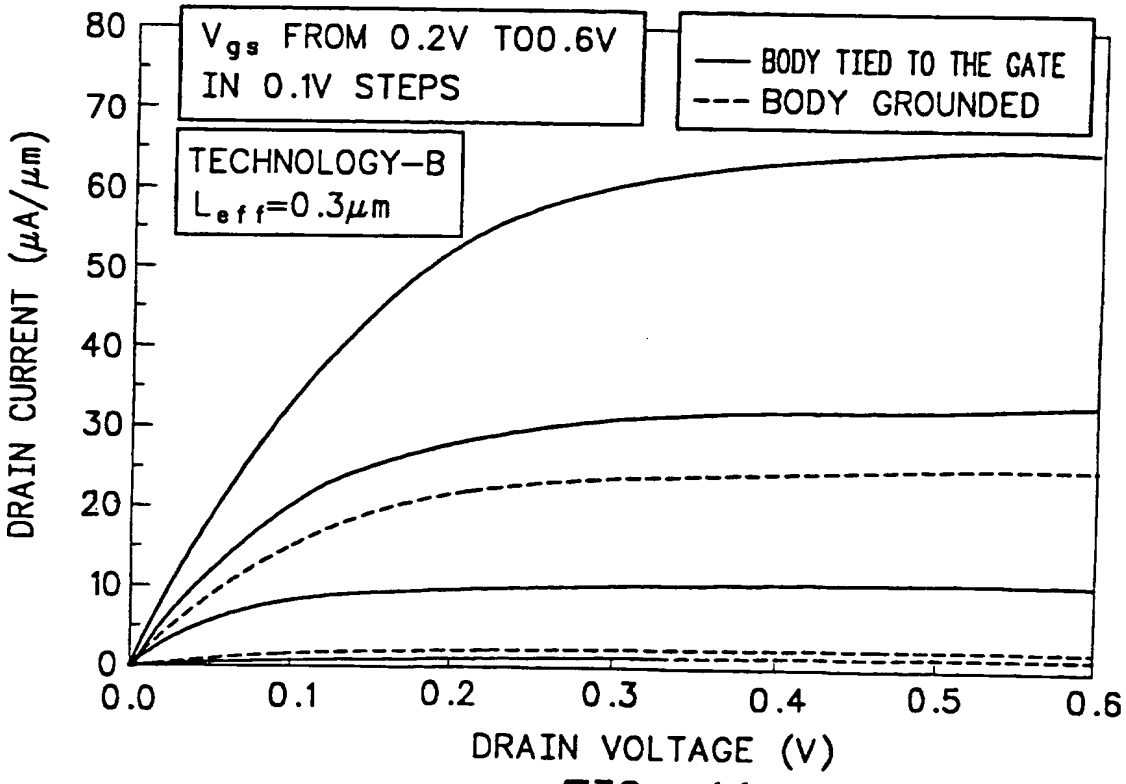


FIG. 11

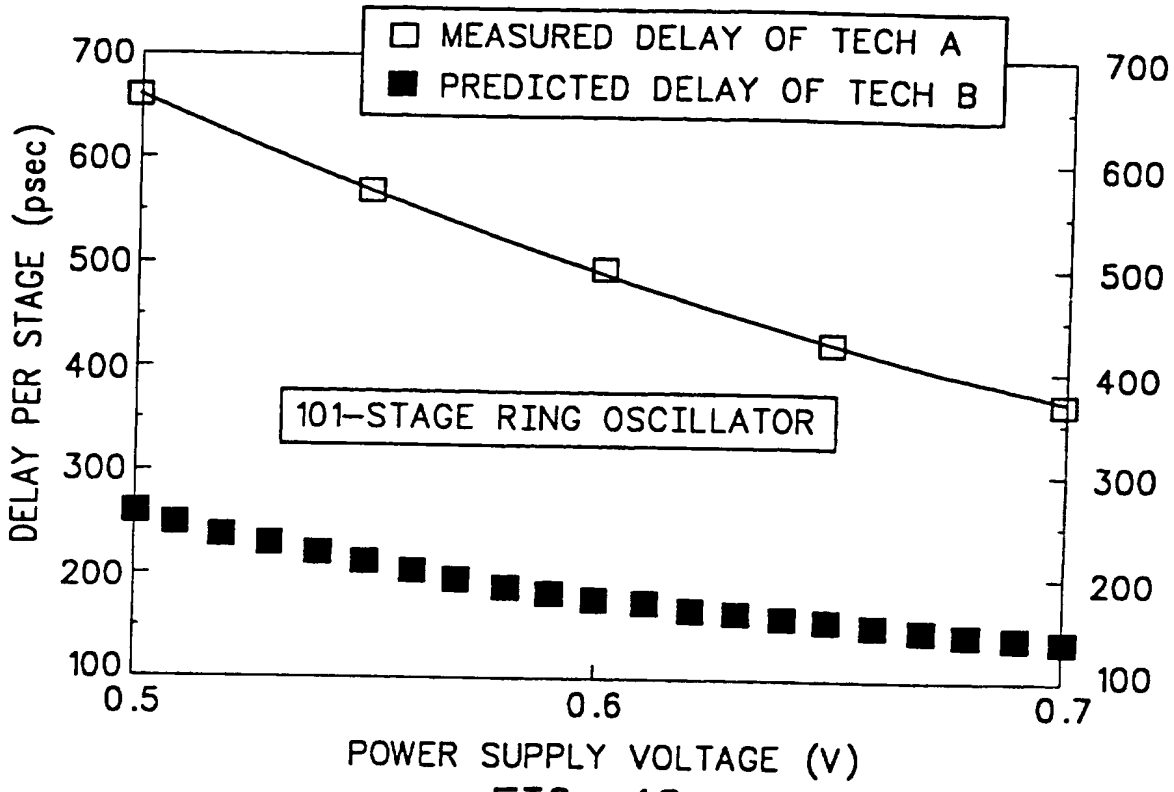


FIG. 12

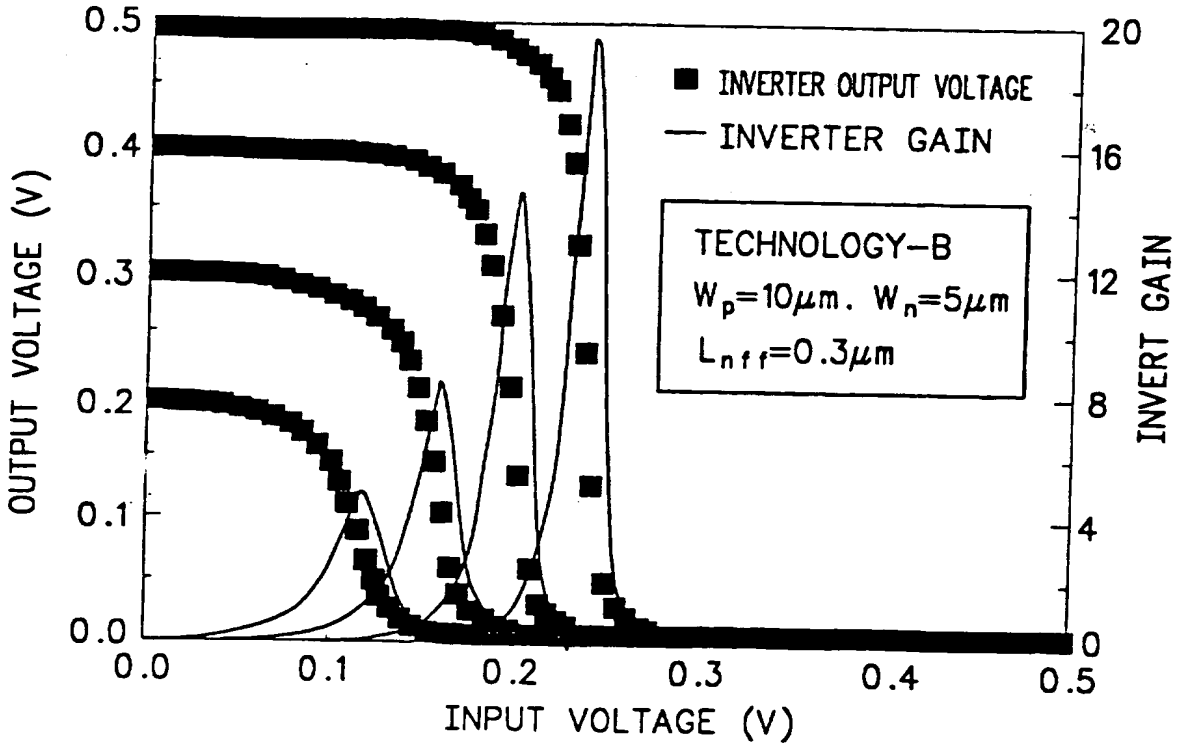


FIG. 13

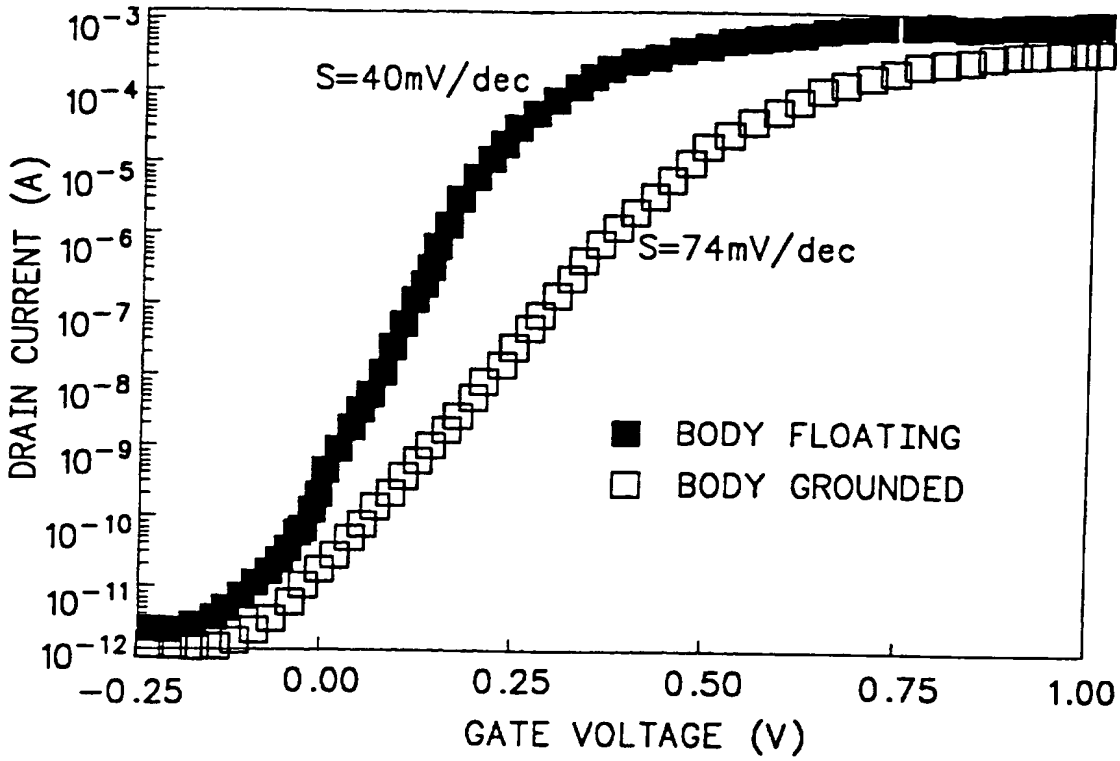


FIG. 14

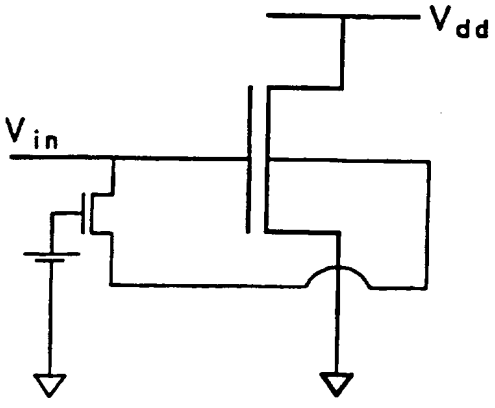


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
US95/06829

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 27/01, 27/12, 29/78,29/80
US CL :257/347,351,384,388,407; 323/315

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/347,348,349,350,351,369,384,388,402,407; 323/312,315

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	VERDONCKT-VANDEBROEK ET AL., "HIGHGAIN LATERAL BIPOLAR ACTION IN A MOSFET STRUCTURE", IEEE TRANS ON ELEC. DEV., VOL. 38, NO. 11, 11/91. SEE ENTIRE DOCUMENT	1,2,12 3,10,11
Y	PARKE ET AL., "BIPOLAR-FET HYBRID-MODE OPERATION OF QUARTER-MICROMETER SOI MOSFET'S", IEEE ELEC. DEV. LET., VOL. 14, NO. 5, 5/93 SEE ENTIRE DOCUMENT	1,4-9
Y	US,A, 5,272,432 (NGUYEN ET AL.), 21 DECEMBER 1993, SEE FIG. 3D" AND LINES 64-68 IN COLUMN 5.	13,14

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 04 JULY 1995	Date of mailing of the international search report 12 JUL 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MINH LOAN TRAN Telephone No. (703) 308-4919

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/06829

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P Y	ASSADERAGHI ET AL., "A NOVEL SILICON-ON-INSULATOR (SOI) MOSFET FOR ULTRA LOW VOLTAGE OPERATION", IEEE SYMPOSIUM ON LOW POWER ELECTRONICS, PAGES 58 AND 59, 10/1994. SEE ENTIRE DOCUMENT	1,2,12 3,10,11

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*